REMARKS

Reconsideration of the application is respectfully requested.

The following issues are addressed in the order they were raised in the Office Action.

Claim Objections

The objections to claims 11, 13 and 14 have been noted, and claims 11 and 13 have accordingly been corrected. In addition, an apparent lack of antecedent basis has been corrected in claim 7.

Claims Rejected Under 35 U.S.C. §112

Claims 11 and 13 stand rejected as being unclear for lacking antecedent basis for certain claim limitations. These have been obviated now since claim 11 has been amended to properly depend from claim 6, and claim 13 has been amended to properly depend from claim 5. Reconsideration of these rejections is therefore respectfully requested.

Claims Rejected Under 35 U.S.C. §103

Claims 1-9 and 11-29 stand rejected as being obvious in view of U.S. Patent No. 5,410,723 to Schmidt ("Schmidt") in view of U.S. Patent No. 7,729,711 to Okamoto ("Okamoto"). Applicants respectfully disagree with the rejection for the following reasons.

Beginning with claim 1, a data driven processing method is recited in which certain operations are performed upon a data driven processor. The data driven processor is understood here to have at least a first processing unit and a second processing unit. Instructions are provided to the first processing unit to operate upon incoming data. A data path for transferring data between the second processing unit and external memory is configured. *The first unit, in response to recognizing that the instructions will require either reading from or writing to external memory, provides*

addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second unit via the configured data path. The Office Action has not made a convincing showing that all limitations of such a method are disclosed in the combination of Schmidt and Okamoto.

The Office Action at pages 3 and 4 refers to Schmidt as meeting all claim limitations of claim 1 except for a processing unit being connected to external memory. First, Applicants respectfully point out that nowhere in the rejection is it explained how Applicants' claim limitations read on corresponding elements or operations in Schmidt and Okamoto. Applicants can appreciate the relevance of Schmidt in that Schmidt discloses a wave front array processor that is data driven, and has a number of individual cells which are interconnected with each other and that can be programmed with instructions for processing incoming data and producing result data. Applicants also understand that Okamoto discloses a data driven processor that can read and write from an external main memory. However, nowhere does Schmidt or Okamoto teach or suggest that *a first processing unit, of the data driven processor, recognize that a set of instructions (which are provided to it to operate upon incoming data) will require either reading from or writing to external memory, **and in response provide addressing information to a memory access unit of the data driven processor to enable the transfer of additional data between the external memory and a second processing unit of the data driven processor, via the configured data path.***

As recognized in the Office Action, Schmidt does not disclose details regarding interfacing with an external memory. While Okamoto does describe how a data driven processor can be interfaced to an external main memory, **the focus there is on the use of an address translation table to maintain a cache coherence between the data driven processor and the external main memory**. Okamoto does not teach or suggest how any one of several processing units (or cells) that make up the data driven processor responds to its programmed instructions, as recited in Applicants' claim 1. Okamoto is only focusing on the interface between the outer periphery of a data driven processor and external memory. The addressing information that is needed is assumed to appear, some how, at the outside interface of the data driven processor. As far as Applicants

are aware, in a conventional data driven processor, a built-in host controller assists the processor by orchestrating the feeding of instructions and incoming data to individual processing elements (processing units) of the data processor. It is also this host controller that identifies sequentially addressed locations in external memory to which, for instance, an outgoing stream of data from the data processor is written. In that situation, a processing element or cell (*processing unit*) of the data driven processor is not aware of the particular address or source of the incoming data, **nor does it know where, that is what address or location in external memory, its result data is ultimately destined**. Okamoto is silent on this issue and therefore lacks the teaching needed to render claim 1 obvious.

Applicants also note the following difficulties with the rejection of claim 1, as recited in pages 3 and 4 of the Office Action. First, although a reference is made to several passages in Schmidt, the Office Action never commits to identifying which limitations of Applicants' claims read on which elements disclosed in Schmidt. For instance, the Office Action could have indicated that Applicants' claimed *first and second processing units* read on the individual cells zp within the array processor of Schmidt. Instead, Applicants are left wondering how the Examiner is interpreting the claims. This fails to provide a constructive environment for determining the allowable scope of claims in an expeditious manner. Accordingly, it is respectfully requested that the Examiner provide more clarity regarding how the limitations of the claims read on which elements of the prior art references being used, so that Applicants are more able to effectively respond to these contentions (not just by argument but also by amending the claims if needed).

As another example, the Office Action merely points to col. 2, lines 20-26 of Schmidt as allegedly reciting Applicants' capability of *the first processing unit, in response to recognizing that the first set of instructions will require reading from or writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data* ... Applicants are left wondering how Schmidt meets this limitation. There is no explanation in the Office Action as to how the following passage taken from Schmidt, col. 2, lines 20-26, meets the relevant claim limitation:

> European Patent Application EP-A O 2277 262 discloses an array processor having a plurality of identical cells in a two-dimensional (mesh) array. Thus, each cell can communicate with four adjacent cells via four communication buses. Data transfer is asynchronous from cell to cell. Each cell contains a data memory, an arithmetic logic unit and a shift register.

The above passage merely refers to a data driven processor with constituent cells that are arranged in a two-dimensional mesh array. It does not refer to how one of the cells, for instance, *in response to recognizing that its programmed instructions will require reading from or writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and another cell of the data processor.* Schmidt simply discloses a data driven processor whose cells communicate with each other, that is, adjacent cells communicate data with each other, using a handshaking protocol. Okamoto discloses a data driven processor that communicates with an external memory through a cache coherent system. Neither reference teaches or suggests how a cell of the data driven processor recognizes that instructions provided to it will require reading from or writing to external memory, and in response provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and another cell (via a data path that has been configured between that other cell and the external memory). Accordingly, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

As to claim 5, neither Schmidt or Okamoto suggest a data processor having a number of processing units coupled to each other as recited in the claim, and wherein *one of the processing units has a control port from which it is to send information to a DMA unit of the data processor about setting up a DMA channel through which data to be consumed or result data by one of the processing units is transferred.* In Schmidt, that handshake ports of adjacent cells communicate with each other to transfer data, between adjacent cells only. In Okamoto, a cache memory unit CM is provided between a memory interface unit VM and a data driven processor PE (see Fig. 5 of Okamoto). A data packet that includes an address of the main memory is provided by the processor, for example, as part of a write or read instruction. However, neither Schmidt nor Okamoto teach or

suggest modifying a cell within the data processor of Schmidt or Okamoto, to provide the cell with *a control port from which it is to send information to a DMA unit about setting up a DMA channel through which data to be consumed or result data by one of the cells is transferred.* Applicants' claim 5 modifies the *processing unit* with the claimed *control port* as recited, making the *processing unit* aware of the location from which data is read to be consumed, or to which result data is to be written, by *sending information to the DMA unit about setting up a DMA channel* through which the data to be consumed or result data by another processing unit is transferred. As neither Schmidt nor Okamoto teach or suggest such capability for a constituent cell of a data driven processor, reconsideration and withdrawal of the rejection is respectfully requested.

As to claim 17, this claim recites a system in which a data driven processor has a memory access unit and a number of processing units having the capability recited, as well as being coupled to each other as recited, where *one of the processing units has a control port which it uses to write data location information to the memory access unit.* Neither Schmidt nor Okamoto teach or suggest that an individual processing cell or unit that makes up a data driven processor be provided with such a capability.

As to claim 23, this claim recites a system in which a data driven processor has a memory access unit and multiple processing units, each coupled to each other as recited, and wherein one of the processing units has *a control port which it uses to write data channel information to the memory access unit.* Neither Schmidt nor Okamoto teach or suggest that an individual processing cell or unit that makes up a data driven processor be provided with such a capability.

Finally, claim 27 is recited in means plus function format and includes a *means for implementing a programmable control path through multiple data consumption means, to transfer higher level read and write commands from one of the data consumption means to a higher level read and write translation means.* Once again, the Office Action does not adequately present the basis for its rejection of this claim, by, for example, mapping the various limitations of Applicants' claim 27 to corresponding elements in the prior art. The Office Action at page 3 merely recites that Schmidt/Okamoto disclose a data processor as recited, referring only to passages in the text that are not helpful in

determining how the Examiner is interpreting the claim limitations. For instance, Applicants are left wondering what elements in the prior art does the limitation *means for implementing a programmable control path through the plurality of data consumption means to transfer higher level read and write commands from one of the data consumption means to the higher level read and write translation means* read on. The Office Action refers to memory instructions of Schmidt/Okamoto that require the use of switching data streams which are considered to be the lower level memory access command. But no conclusion can be drawn from that statement. These "memory instructions" described in Schmidt are different than those that are of concern in Okamoto. The instructions in Okamoto are designed to interface the data driven processor to external memory. The instructions in Schmidt are designed to program individual cells. There needs to be further explanation of how a person having ordinary skill in the art would understand such instructions as being used in the manner recited in Applicants' claim 27. No such explanation has been given in the Office Action. Accordingly, it is respectfully submitted that the case made for rejecting the claims in the Office Action is improper in that it does not fairly apprise Applicants of the basis for the rejection.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language, including the right to swear behind or otherwise remove an improper art reference.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: December 27, 2007.

By _____
Farzad E. Amini, Reg. No. 42,261

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(310) 207-3800

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on December 27, 2007.

_____
Margaux Rodriguez *December 27, 2007*